Viasat’s ECC66100 is a family of soft decision Forward Error Correction (FEC) IP cores based on Turbo Product Code (TPC) designed for use in 100 Gbps communications applications.

TPCs are the optimum FEC for high data rate applications as they provide high Net Electrical Coding Gain (NECG) with low implementation complexity. TPCs also have large minimum distances leading to a very low error floor, several orders of magnitude below the target 1e-15 Bit Error Rate (BER), based on asymptotic analysis.

ECC6100’s underlying TPC architecture has been used extensively for a variety of applications that has proven successful in both simulations and hardware.

The ECC6100 series consists of the following overhead rates:

- 15% with 11 dB NECG
- 20% with 11.3 dB NECG
SPECIFICATIONS

FEATURE/PARAMETER

Coded Line Rate
- 15% OH: 120 Gbps
- 20% OH: 126 Gbps

NECG
- 15% OH: 11 dB
- 20% OH: 11.3 dB

Clocking: 500 MHz

Burst Error Correction
- 15% OH: 1536
- 20% OH: 1152

Soft Decision Resolution
- 4 bits
- LLR input 8 bits I & Q

Latency
- Encoder
  - 15% OH: 2 µs
  - 20% OH: 1 µs
- Decoder
  - 15% OH: less than 8 µs
  - 20% OH: 5 µs

FEATURE/PARAMETER (CONTINUED)

Power Consumption: 40 nm process <8 W Typical

Size (Includes Flipflops, Logic Gates and RAM)
- Encoder + interleaver
  - 15% and 20% OH: 1.64 M equivalent gates
- Decoder + deinterleaver
  - 15% OH: 25.8 M equivalent gates
  - 20% OH: 22.0 M equivalent gates

DELIVERABLES
- Encrypted RTL: synopsys and/or cadence compatible
- System verilog, VMM based testbench and testcases
- “C” SW model (gcc object file)
- User documentation

RELATED VIASAT PRODUCTS
- DSP IP cores for coherent receiver and transmitter
- FPGA demonstration platform for algorithm verification

Visit www.viasat.com for further information

FIGURE 1. TPC DECODER

FIGURE 2. TPC ENCODER