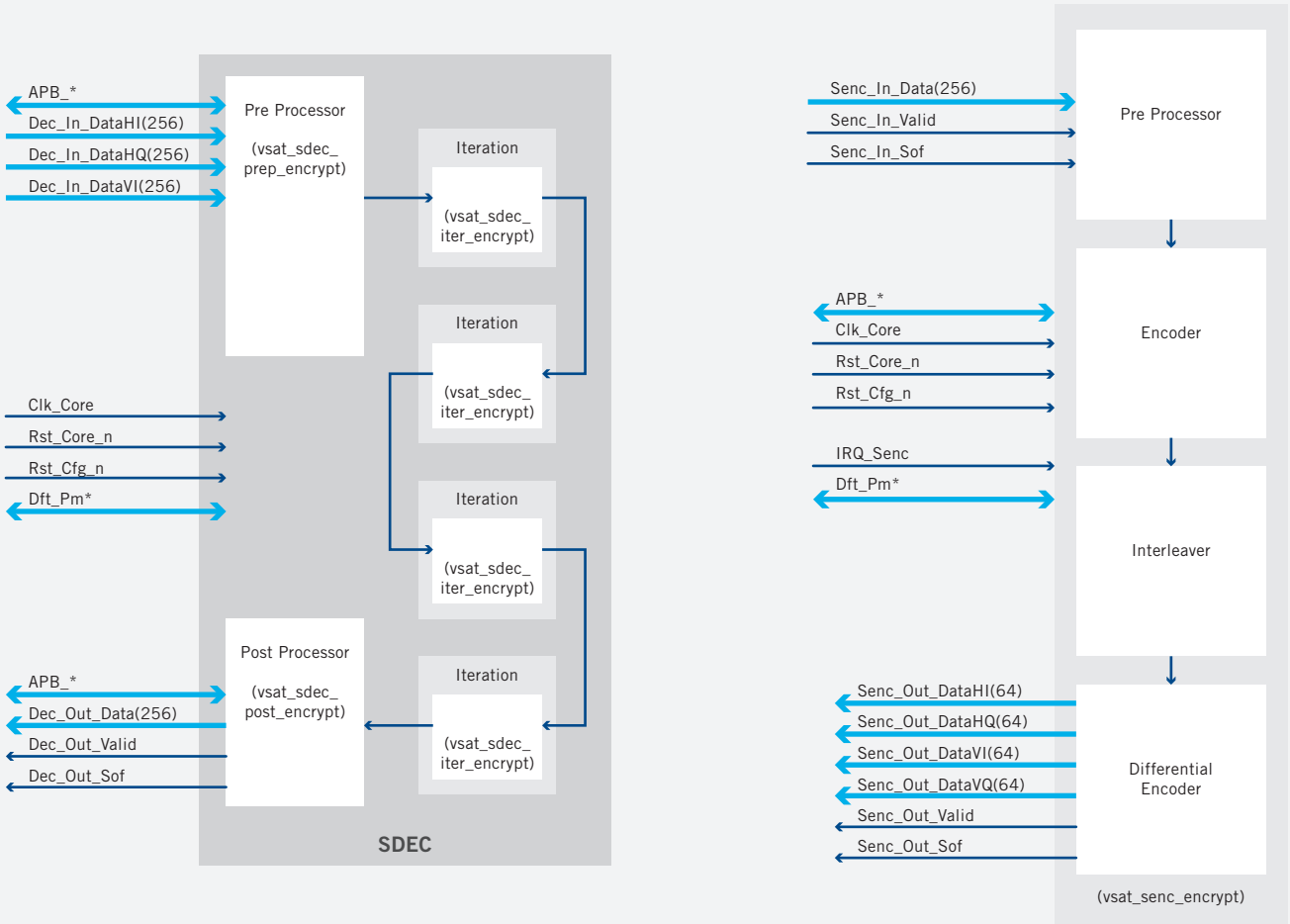
Viasat SDFEC 66200
200 Gbps SDFEC

Viasat 66200 SDFEC (Soft Decision Forward Error Correction) is a family of turbo product code (TPC) designed for use in 200 Gbps communications applications. The multi rate SDFEC handles BPSK, QPSK, and 16-QAM modulation formats. With either 7% or 20% overhead, TPCs are the optimum FEC for high data rate, high coding gain applications where low latency and high net equivalent coding gain (NECG) are desired.

TPC's have large minimum distances leading to a very low error floor, which is desired for 200 Gbps optical network applications. Further, TPCs have low complexity while achieving high performance. The 66200 series of cores are based on a soft decision TPC code that Viasat has used extensively for a variety of applications; hence the architecture is well tested in both simulations and hardware.

The NECG of 20% overhead TPC code is 11.3 dB for coherent QPSK modulation in an AWGN channel at $1x10^{-15}$ BER. The 7% overhead TPC code has an NECG of 10.2 dB. Asymptotic analysis reveals that the error floor is more than five orders of magnitude below the $1x10^{-15}$ BER performance target.

REPRESENTATIVE BLOCK DIAGRAM OF DECODER & ENCODER



SPECIFICATIONS

FEATURE/DETAILS

Baud Rate	~32 GBaud
Modulation Configurability	Switchable between » PM-BPSK » PM-DBPSK » PM-QPSK » PM-DQPSK » PM-16QAM » PM=D16QAM
Line Rates	~64 Gbps, ~128 Gbps and ~256 Gbps for (D)BPSK, (D)QPSK and (D)16-QAM respectively.
FEC Overhead	7.8% and 20.5% configurable
Differential Encoding	Supports multiple pre-coding methods as well as bypass
SDFEC Decoder Bypass	Supported for channel BER monitoring

PERFORMANCE

20% SDFEC NECG @ 10^{-15} BER	11.3 dB (QPSK)
20% SDFEC Eb/No @ 10^{-15} BER	» PM-BPSK: 3.7 dB » PM-DBPSK: 4.8 dB » PM-QPSK: 3.7 dB » PM-DQPSK: 4.8 dB » PM-16QAM: 7.2 dB » PM-D16QAM: 8.3 dB
7% SDFEC NECG @ 10^{-15} BER	10.2 dB (QPSK)
7% SFDEC Eb/No @ 10^{-15} BER	» PM-BPSK: 4.8 dB » PM-DBPSK: 5.5 dB » PM-QPSK: 4.8 dB » PM-DQPSK: 5.5 dB » PM-16QAM: 8.5 dB » PM-D16QAM: 9.2 dB
Burst Error Correction Capability	1152 Bits
Decoder Latency	» 3 µs for 20% OH (200 Gbps) » 14 µs for 7% OH (200 Gbps)

INTERFACES

Data Interfaces	Simple handshaking with valid, data, start and end
Processor Interface	APB interface for control and monitoring
SDFEC Input Resolution	9-bits I and 9-bits Q

IMPLEMENTATION

Clocking	500 MHz
Power Dissipation (TSMC 28 nm)	» PM-DBPSK: 8 W » PM-DQPSK: 10 W » PM-D16QAM: 14 W
Number of Gates	» 45 million NAND-2 gate equivalents (logic) » 45 million NAND-2 gate equivalents (RAM)
Silicon Area (TSMC 28 nm)	34 mm^2
Design Partitioning	Supported for easier back end integration

CONTACT

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